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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,246	04/01/2004	Takahiro Okuno	251363US2	6970

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,246	OKUNO ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6, and 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (US Pub. No. 2003/0042525), hereinafter Tanaka.

3. A copy of Fig. 13 from Tanaka is provided with additional references to clarify comparisons made by the examiner. The figure is identical to the original figure from Tanaka, with the exception that six new reference labels have been added.

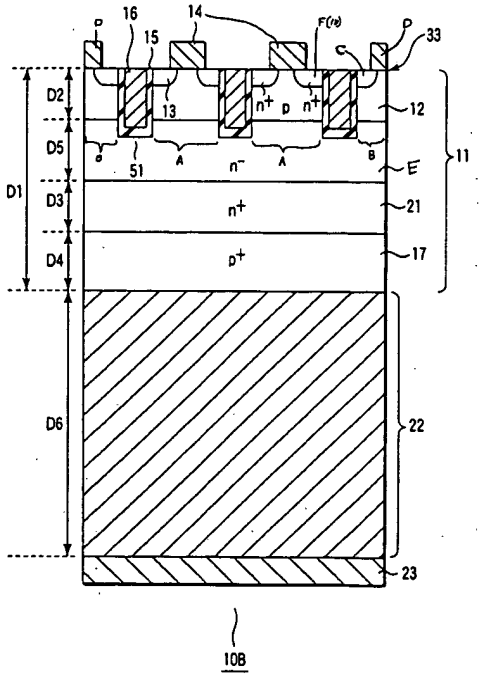

FIG. 13

4. Regarding claims 1 and 8, Tanaka discloses (Fig 13) a semiconductor device comprising:

a drift layer (E) of a first conductivity type;

a collector layer (17) of a second conductivity type located on the drift layer;

a collector electrode (22,23) located on the collector layer;

a base layer (12) of the second conductivity type located in a region isolated from the collector layer on the drift layer;

a plurality of trenches (51) formed at certain intervals to extend from the top surface of the base layer into the drift layer and thereby divide the base layer to main cell regions (A) and dummy cell regions (B);

a first emitter layer (F, 13) of the first conductivity type selectively formed in the surface layer of the base layer in each main cell region to extend along adjacent one of the trenches;

gate electrodes (16) formed in the trenches sandwiching each main cell region among said plurality of trenches via a gate insulating film (15);

an emitter electrode (14) located over the base layer and the first emitter layer in each main cell region; and

a second emitter layer (C) of the first conductivity type selectively formed so as to be scattered in the surface layer of the base layer in each dummy region and having a surface area smaller than that of the first emitter layer (Note that Fig. 13 clearly shows second emitter layer (C) smaller than first emitter (F). With respect to this comparison,

drawings may not be interpreted as providing exact dimensions, but may be interpreted to indicate relative sizes).

5. Further regarding claim 8, Tanaka inherently discloses "wherein resistance value of a floating resistor as a resistance between the base layer or the dummy cell region and the emitter electrode is adjusted to be smaller than the resistance value causing rise of the gate-emitter voltage due to negative capacitance of the gate in a period to charge a gate charge between the gate and the collector by a voltage applied between the gate and the emitter when the device is turned on." Since Tanaka discloses the same structure as the applicant's, it functions similarly.

6. Regarding claims 2 and 9, Tanaka inherently discloses the drift layer of the main cell region has a carrier concentration profile having a peak on the side of the first emitter layer (it is known to one of ordinary skill in the art that the impurity implantation process by nature provides an impurity concentration profile having a peak on the implantation side, the side of the first emitter).

7. Regarding claims 3 and 10, Tanaka inherently discloses:

the drift layer of the main cell region forms a current path narrow enough to accumulate a carrier of the second conductivity type on and around the bottom of the trenches when the device is turned on, and

wherein the second emitter layer forms a current path conducting a carrier of the second conductivity type to the emitter electrode by an amount no affecting the injection efficiency of the carrier of the first conductivity type from the emitter electrode to the drift

layer when the device is turned on (since Tanaka discloses the same structure as the applicant's, it functions similarly).

8. Regarding claims 4 and 12, Tanaka inherently discloses wherein the second emitter layer is formed as isolated patterns in contact with the trenches opposed to each other via the base layer in each dummy cell region (it is known to one of ordinary skill in the art that the manufacture of semiconductor devices such as Tanaka's and the applicant's results in a layout in which cross-sections like Tanaka's Fig. 13 or applicant's Fig. 2 are repeated in a lateral direction).

9. Regarding claims 6 and 11, Tanaka discloses (Fig 13) a via contact (D) formed in contact with the second emitter layer (C) to connect the base layer (12) in the dummy cell region (B) to the emitter electrode (14) via the second emitter layer,"

Additionally, Tanaka discloses "wherein the resistance value of a floating resistor as a resistor between the base layer of the dummy cell region and the emitter electrode is adjusted by geometries of the second emitter layer and the via contact", due to the mere presence of the claimed structure.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 5, 7, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka.

12. Regarding claims 5 and 13, Tanaka discloses (Fig 13) the semiconductor devices having the second emitter layer (D) formed as patterns in contact with the trenches (51) opposed to each other via the base layer in each dummy cell region. Tanaka differs from the claimed invention only in not expressly disclosing "the second emitter layer is formed as island shaped patterns each having opposite ends in contact with the trenches." However, such difference is regarded as nothing more than an obvious variation of Tanaka. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to connect the isolated second emitter regions opposing one another in each dummy cell region to one another, forming a continuous island-pattern second emitter region with opposite ends in contact with the trenches opposed to each other; at least for enhanced electrical effect of second emitter region, enlarging the second emitter region.

13. Regarding claims 7 and 14, Tanaka differs from the claimed invention only in not disclosing "the resistance value of the floating resistor is 0.3Ω – 3Ω when the applied voltage between the collector and the emitter is 600V and the gate resistance is 51Ω". However, such difference is regarded as nothing more than an obvious design choice. That is, varying parameters such as size, concentration, and resistivity merely requires routine experimentation. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to adjust the resistance value of the floating

resistor to between 0.3Ω – 3Ω when the applied voltage between the collector and the emitter is 600V and the gate resistance is 51Ω; at least for device stability.

Response to Arguments

14. Applicant's amendments to the title, specification, and abstract, are accepted as not adding new matter. Accordingly, the objections to the title, specification, and abstract, are withdrawn.

15. Applicant's arguments regarding the requirement to submit a further cross-sectional view are persuasive. Examiner concurs that the subject matter regarding claims 5 and 13 is adequately shown in Figures 7-10 as supported by the corresponding disclosure in the specification. Accordingly, the outstanding objection is withdrawn.

16. Applicant's arguments filed 10/27/2005 regarding the rejection of Claims 1-14 based on Tanaka have been fully considered but they are not persuasive.

17. Examiner does not concur that "Tanaka fails to disclose or obviate" the common fundamental feature of Claims 1 and 8 "that a base layer of the second conductivity type is divided into main cell regions and dummy cell regions." Nothing in the claims and no submitted evidence precludes the labeling of main (A) and dummy (B) cell regions in Fig 13 of Tanaka. The claims fail to structurally distinguish over the cited art.

18. Examiner does not concur that "Tanaka neither discloses or suggests" the feature of Claim 8 regarding the resistance value of a floating resistor. Tanaka inherently discloses this functional property of the claimed structure in disclosing an identical structure.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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